LISTING OF CLAIMS SN 10/014,928

CLAIMS 1-22 (Cancelled)

43. (Currently Amended) A method of operating a dual-die, double-sized, back-to-back integrated-circuit chip assembly, comprising the steps of:

mounting a pair of integrated-circuit chips back-to-back, where each integrated-circuit chip has one or more pairs of reversible wire-bonding pads; and

electrically reversing internal connections to the wire-bonding-pads on one of the integrated-circuit chips so that pads on each integrated-circuit chip for similar functions are located near each other for wire-bonding so that identical integrated-circuit chips are used to provide the dual-die, double-sized, back-to-back integrated-circuit chip assembly;

applying an external voltage to a bonding-option wire-bonding-pad to indicate whether the integrated-circuit chip is to provide a standard pattern for the reversible wire-bonding-pads, or alternatively, whether the integrated-circuit chip is to provide a reversed path for the reversible wire-bonding-pads; and

sensing the voltage applied to the bonding-option wire-bonding-pad for alternatively generating either a standard NRO gate control signal or a non-standard, reversed RO gate control signal from the voltage state of the bonding-option wire-bonding-pad.

44. (Original) The method of Claim 43 including fabricating the two integrated-circuit chips with the same mask sets.

45. (Original) The method of Claim 43 wherein the step of electrically reversing the internal connection to the wire-bonding-pads of one of the integrated-circuit chips includes the steps of:

selectively connecting a first wire-bonding-pad to the internal circuits usually connected to internal circuits for a second wire-bonding-pad; and

selectively connecting a second wire-bonding-pad to the internal circuits usually connected to internal circuits for the first wire-bonding-pad.

46. **(Currently Canceled).**

47. (Original) The method of Claim 43, including the steps of:

applying an external voltage to two or more bonding-option wire-bonding-pads;

respectively sensing the voltage applied to a respective bonding-option wire-bonding-pad;

generating one or more bonding option logic signals; and

generating standard NRO and non-standard, reversed RO gate control signals from the one or more bonding option logic signals.

48. (Original) The method of Claim 43 including the step of fabricating the first and the second chips with the same mask sets to provide identical integrated-circuit chips and wherein internal connections of one of said pair of integrated-circuit chips are electrically reversed when assembled back-to-back to the other chip of the identified pair such that the pads for similar functions are located near each other for wire-bonding to a common bonding finger of said lead frame.

49. (Original) A method of providing a dual-die, double-sized, back-to-back integrated-circuit chip assembly, comprising the steps of:

providing a first and a second integrated-circuit chip, each having one or more electrically reversible wire-bonding-pads;

centrally mounting the first and the second integrated-circuit chips back-to-back within a lead frame having inwardly-extending bonding fingers with one of said chips having its wire-bonding-pads electrically reversed such that the pads for similar functions are located near each other for wire-bonding to a common bonding finger of said lead frame; and

for each integrated-circuit chip:

connecting an input signal terminal of a first gate circuit to a first wire-bonding-pad, connecting an output signal terminal of the first gate circuit to a first common signal line, and receiving a standard wire-bonding configuration control signal at a control terminal of the first gate circuit, which control signal operates the first gate circuit to provide a standard pattern for the first wire-bonding-pad, which standard pattern connects the first wire-bonding-pad to a first common signal line to thereby provide a first input LOGIC signal to the first common signal line on said integrated-circuit chip;

connecting an input signal terminal of a second gate circuit to the first wire-bonding-pad, connecting an output signal terminal of the second gate circuit to a second common signal line, and receiving a non-standard, reversed wire-bonding configuration control signal at a control terminal of the second gate circuit, which control signal operates the second gate circuit to alternatively provide a non-standard, reversed pattern for the first wire-bonding-pad, which non-standard, reversed pattern connects the first wire-bonding-pad to a second common signal line to thereby alternatively provide the first input LOGIC signal to the second common signal line on said integrated-circuit chip;

connecting an input signal terminal of a third gate circuit to a second wire-bonding-pad, connecting an output signal terminal of the third gate circuit to a second common signal line, and receiving the standard wire-bonding configuration control signal at a control terminal of the third gate circuit, which control signal operates the third gate circuit to provide a standard pattern for the second wire-bonding-pad, which standard pattern connects the second wire-bonding-pad to a second common signal line to thereby provide a second input LOGIC signal to the second common signal line on said integrated-circuit chip;

connecting an input signal terminal of a fourth gate circuit to the second wire-bonding-pad, connecting an output signal terminal of the fourth gate circuit to the second common signal line, and receiving the non-standard, reversed wire-bonding configuration control signal at a control terminal of the fourth gate circuit, which control signal operates the fourth gate circuit to alternatively provide a non-standard, reversed pattern for the second wire-bonding-pad, which non-standard, reversed pattern connects the

second wire-bonding-pad to the first common signal line to thereby alternatively provide the second input LOGIC signal to the first common signal line on said integrated-circuit chip;

wherein the first gate circuit and the third gate circuit are controlled by the standard-bonding-pad control signal to provide a predetermined standard bonding-pad configuration for the integrated-circuit chip, which standard bonding-pad configuration connects the first wire-bonding input pad to the first common signal line on the integrated-circuit chip and which standard bonding-pad configuration also connects the second wire-bonding-pad to the second common signal line; and

wherein the second gate circuit and the fourth gate circuit are controlled by the reverse-bonding-pad control signal to provide a predetermined alternative reversed bonding-pad configuration for the integrated-circuit chip, which alternative reversed bonding-pad configuration connects the first wire-bonding-pad to the second common signal line and which alternative reversed bonding-pad configuration also connects the second wire-bonding-pad to first common signal line.

50. (Original) The method of Claim 49 including:

applying an external voltage to a bonding-option wire-bonding-pad to indicate whether the integrated-circuit chip is to provide a standard pattern for the reversible wire-bonding-pads, or alternatively, whether the integrated-circuit chip is to provide a reversed path for the reversible wire-bonding-pads; and

sensing the voltage applied to the bonding-option wire-bonding-pad for alternatively generating either a standard NRO gate control signal or a non-standard, reversed RO gate control signal from the voltage state of the bonding-option wire-bonding-pad.

51. (Original) The method of Claim 50 including:

applying an external voltage to two or more bonding-option wire-bonding pads;

sensing the voltage applied to a respective bonding-option wire-bonding pad;

generating one or more bonding option logic signals; and

generating standard NRO and non-standard, reversed RO gate control signals from one or more bonding option logic signals.

52. (Original) The method of Claim 51 including applying an external voltage to three bonding-option wire-bonding-pads such that the logic circuit for generating standard NRO and non-standard, reversed RO gate control signals generates the standard NRO and non-standard, reversed RO gate control signals.

53. (Original) The method of Claim 49 including connecting with a logic circuit a first signal input terminal to one of the wire-bonding-pads, the logic circuit receiving a second control signal input to operate the gate circuit, and coupling an output terminal of the logic circuit to one of the common signal lines.

54. (Original) The method of Claim 53 wherein the gate circuits including receiving a chip enable signal CE to activate the gate circuits

55. (Original) The method of Claim 53 wherein the logic circuit includes a first logic gate, having an input terminal connected to a first signal input terminal, having a second input terminal connected to the second control signal input terminal, and having an output terminal connected to an input terminal of the output driver circuit; and

wherein the logic circuit includes a second logic gate, having an input terminal connected through an inverter to the first signal input terminal, having a second input terminal connected through an inverter to the second control signal input terminal, and having an output terminal connected to an input terminal of the output driver circuit.

56. (Original) The method of Claim 55 wherein the first logic gate includes a NAND gate and wherein the second logic gate includes a NOR gate.

57. (Original) The method of Claim 56 including receiving a chip enable signal CE at a first input terminal of the first logic gate and receiving an inverted chip enable signal at the input terminal of the second logic gate.

58. (Original) The method of Claim 57 wherein the logic circuit includes an output driver circuit having an input terminal and having an output terminal connected to one of the common signal lines.

59. (Original) The method of Claim 49 wherein the first and the second wire-bonding-pads are adapted to be connected to external control signals for the integrated-circuit chip.

60. (Original) The method of Claim 49 wherein the first and the second chip are fabricated with the same mask sets to be identical chips and wherein one of said pair of identical chip are reversed when assembled back-to-back to the other chip of the identified pair such that the pads for similar functions are located near each other for wire-bonding to a common bonding finger of said lead frame.

61. (Original) A method of providing a dual-die, double-sized, back-to-back, wire-bonded integrated-circuit chip assembly, comprising:

providing a first chip having one or more reversible wire-bonding-pads; and

providing a second chip having one or more reversible wire-bonding-pads;

centrally mounting back-to-back the first and second integrated-circuit chips within a lead frame having inwardly-extending bonding fingers with one of said chips having its wire-bonding-pads electrically reversed such that the pads for similar functions are located near each other for wire-bonding to a common bonding finger of said lead frame;

applying an external voltage to a bonding-option wire-bonding-pad adapted to indicate whether the integrated-circuit chip is to provide a standard pattern for the reversible wire-bonding-pads, or alternatively, whether the integrated-circuit chip is to provide a reversed path for the reversible wire-bonding-pads; and

sensing the voltage applied to the bonding-option wire-bonding-pad for alternatively generating either a standard NRO gate control signal or a non-standard, reversed RO gate control signal from the voltage state of the bonding-option wire-bonding-pad.

62. (Original) The method of Claim 61 including fabricating the first and the second chip with the same mask sets to provide identical chips, wherein one of said pair of identical chip is electrically reversed when assembled back-to-back to the other chip of the identified pair such that the pads for similar functions are located near each other for wire-bonding to a common bonding finger of said lead frame.